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2823

D900D PATENT

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Plat et al.
Serial No.:	10/079,775
Filed:	February 12, 2002
Group Art Unit:	2823
Before the Examiner:	Lee, Hsien Ming
Title:	A METHOD FOR REDUCING ANTI-REFLECTIVE COATING LAYER REMOVAL DURING REMOVAL OF PHOTORESIST

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc., which is the assignee of the entire right, title and interest in the above-identified patent application.

03/22/2005 HALI11 00000007 010365 10079775
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CERTIFICATION UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on March 18, 2005.

Serena Beller
Signature

Serena Beller
(Printed name of person certifying)

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-6 and 13-18 are pending in the Application. Claims 4-6 and 13-18 are allowed. Claims 1-3 stand rejected. Claims 1-3 are appealed.

IV. STATUS OF AMENDMENTS

The Appellants' response to the Office Action having a mailing date of October 8, 2004, has been considered, but the Examiner indicated that it did not place the application in condition for allowance because Appellants' arguments were deemed unpersuasive.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In one embodiment of the present invention, a method of providing a semiconductor device, the semiconductor device including a first layer desired to be etched, may comprise providing an anti-reflective coating layer having antireflective properties, wherein the anti-reflective coating layer comprises a layer of SiON having a thickness of less than about 500 Angstroms (Å) deposited on the first layer. Specification, page 11, lines 12-19; Specification, page 16, claim 1; Figure 4B, steps 112, 114; Figure 5A, elements 214, 212. The method may further comprise patterning a resist layer, the resist layer including a pattern having a plurality of apertures therein for etching a first portion of the first layer. Specification, page 11, line 19-page 12, line 1; Specification, page 16, claim 1; Figure 4B, step 116; Figure 5A, element 216. The method may further comprise etching the first portion of the

first layer. Specification, page 12, line 4; Specification, page 16, claim 1; Figure 4B, step 118. The method may further comprise removing the resist layer utilizing a plasma etch, the anti-reflective coating layer being resistant to the plasma etch. Specification, page 12, lines 4-8; Specification, page 16, claim 1; Figure 4B, step 120; Figure 5B, element 214. The method may further comprise patterning a second resist layer, the second resist layer including a pattern having a plurality of apertures therein for etching a second portion of the first layer. Specification, page 12, lines 16-23; Specification, page 16, claim 1; Figure 4B, step 124. The method may further comprise etching the second portion of the first layer. Specification, page 12, line 23-page 13, line 2; Specification, page 16, claim 1; Figure 4B, step 126.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Chung et al. (U.S. Patent No. 6,184,142) in view of Appellants' Background.

VII. ARGUMENT

The Examiner has rejected claims 1-3 under 35 U.S.C. §103(a) as being unpatentable over Chung in view of Appellants' Background. Paper No. 14, page 2. Appellants respectfully traverse these rejections for at least the reasons stated below.

A. Claims 1-3 are patentable over Chung in view of Appellants' Background since the Examiner has not provided any objective evidence or source of motivation for modifying Chung with Appellants' Background.

A prima facie showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to

make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner's motivation for modifying Chung with Appellants' Background to pattern a resist layer where the resist layer includes a pattern having a plurality of apertures therein for etching a portion of a layer desired to be etched, as recited in claim 1 is "since by this manner it would provide a ground for the subsequent processing steps in forming plural gate stacks." Paper No. 12, page 3; Paper No. 14, page 3. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The motivation to modify Chung with Appellants' Background must come from one of three possible sources: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner has not provided any evidence that his motivation comes from any of these sources. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 1-3.

In response to Appellants assertion that the Examiner has not provided evidence that his motivation comes from any of the above-stated sources, the Examiner asserts that his "motivation comes from the source of common knowledge of persons of ordinary skill in the art." Paper No. 14, page 4. Appellants respectfully

contest the assertion that the Examiner does not have to provide any evidence to support a suggestion or motivation for combining references. The Examiner must provide independent evidence to support the assertion that the suggestion to combine references comes from the knowledge and common sense of ordinary skill in the art. *Smiths Industries Medical Systems Inc. v. Vital Signs Inc.*, 51 U.S.P.Q.2d 1415, 1421 (Fed. Cir. 1999). The reliance on "common knowledge and common sense" may not be substituted for evidence. *In re Lee*, 61 U.S.P.Q.2d 1430, 1435 (Fed. Cir. 2002). The Federal Circuit in *In re Lee* specifically held that *In re Bozak* (case that Examiners typically cite to support the assertion that motivation can come from the common knowledge of persons of ordinary skill in the art) did not hold that that common knowledge and common sense are a substitute for evidence. *Id.* Nor does *In re Bozak*, after thirty-two years of isolation, outweigh the dozens of rulings of the Federal Circuit and the Circuit of Customs and Patent Appeals that determination of patentability must be based on evidence. *Id.* The Examiner must submit objective evidence in support of combining references. *In re Lee* at 1434; *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1316-17 (Fed. Cir. 2000). The factual question of motivation is material to patentability and cannot be resolved on subjective belief and unknown authority. *In re Lee* at 1434. Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 1-3.

Furthermore, the Examiner's conclusion of obviousness is based on improper hindsight reasoning. The Examiner's motivation "since by this manner it would provide a ground for the subsequent processing steps in forming plural gate stacks" appears to have been gleaned from Appellants' disclosure. In fact, the Examiner points out that Appellants' Background teaches a resist layer with a plurality of apertures in order to form a plurality of gates stacks. Any judgment on obviousness must not include knowledge gleaned from Appellants' disclosure. *In re McLaughlin*, 170 U.S.P.Q. 209, 212 (C.C.P.A. 1971). Consequently, the Examiner's motivation is

insufficient to support a *prima facie* case of obviousness for rejecting claims 1-3. M.P.E.P. §2145.

Furthermore, the Examiner has not provided any objective evidence as to why one of ordinary skill in the art would modify Chung to pattern a resist layer to have a plurality of apertures therein (Examiner admits that Chung does not teach this limitation) in order to form a plurality of gate stacks (Examiner's motivation). *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Chung specifically teaches forming a single via which requires a single aperture and not a plurality of apertures in the photoresist. Column 2, lines 49-57; Figures 6A-F. Instead, the Examiner merely relies upon his own subjective opinion which is insufficient to establish a *prima facie* case of obviousness. *Id.* Consequently, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1-3. *Id.*

As a result of the foregoing, Appellants respectfully assert that the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1-3. M.P.E.P. §2143.

B. Chung and Appellants' Background, taken singly or in combination, do not teach or suggest the following claim limitations.

1. Claim 1 is patentable over Chung in view of Appellant's Background.

Appellants respectfully assert that Chung and Appellants' Background, taken singly or in combination, do not teach or suggest "removing the resist layer utilizing a plasma etch, the anti-reflective coating layer begin resistant to the plasma etch" as recited in claim 1. The Examiner cites to column 1, lines 52-67 of Chung as teaching or suggesting the above-cited claim limitation. Paper No. 10, page 4. Appellants respectfully traverse the assertion that Chung teaches or suggests the above-cited claim limitation.

Chung instead teaches that a type of low k organic silicon-oxide film with lower carbon-content showed better resistance to pure O_2 plasma during photoresist strip steps. Column 1, lines 57-60. However, the Examiner had previously cited cap layer 114 of Chung as teaching an anti-reflective coating layer. Paper No. 12, page 2; Paper No. 14, page 2. Chung further teaches that stop layer 114 is an etch barrier film such as silicon nitride to prevent the upper trench patterns of dual damascene from being etched through. Column 4, lines 24-26. Chung further teaches that other barrier layers may be used such as silicon oxynitride as long as it has different etch characteristics than low k organic dielectric film and can be used as ARC layer. Column 4, lines 28-31. Chung further teaches that stop layer 114 allows a selective etch process with respect to different underlying materials and also eliminates reflection of incident light. Column 4, lines 31-33. Hence, Chung teaches that stop layer 114 is to have different etch characteristics than low k organic dielectric films. Chung further teaches that the low k organic dielectric films, such as layers 113 and 112 beneath stop layer 114, may have some resistance to pure O_2 plasma. However, Chung does not teach or suggest that stop layer 114 is resistant to a plasma etch. Therefore, the Examiner has not presented a *prima facie* case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

2. Claim 2 is patentable over Chung in view of Appellants' Background for at least the reasons claim 1 is patentable over Chung in view of Appellants' Background.

Claim 2 recites combinations of features including the combinations recited in claim 1 and thus is patentable over Chung in view of Appellants' Background for at least the reasons claim 1 is allowable.

3. Claim 3 is patentable over Chung in view of Appellant's Background.

Appellants respectfully assert that Chung and Appellants' Background, taken singly or in combination, do not teach or suggest "performing the plasma etch using a plasma including a forming gas, the anti-reflective coating layer being resistant to the plasma etch using the plasma including the forming gas" as recited in claim 3. The Examiner cites to column 1, lines 52-67 of Chung as teaching or suggesting an anti-reflective coating layer being resistant to a plasma etch using the plasma including the forming gas. Paper No. 10, page 4. Appellants respectfully traverse the assertion that Chung teaches or suggests the above-cited claim limitation.

As stated above, Chung instead teaches that a type of low k organic silicon-oxide film with lower carbon-content showed better resistance to pure O_2 plasma during photoresist strip steps. Column 1, lines 57-60. However, the Examiner had previously cited cap layer 114 of Chung as teaching an anti-reflective coating layer. Paper No. 12, page 2; Paper No. 14, page 2. Chung further teaches that stop layer 114 is an etch barrier film such as silicon nitride to prevent the upper trench patterns of dual damascene from being etched through. Column 4, lines 24-26. Chung further teaches that other barrier layers may be used such as silicon oxynitride as long as it has different etch characteristics than low k organic dielectric film and can be used as ARC layer. Column 4, lines 28-31. Chung further teaches that stop layer 114 allows a selective etch process with respect to different underlying materials and also eliminates reflection of incident light. Column 4, lines 31-33. Hence, Chung teaches that stop layer 114 is to have different etch characteristics than low k organic dielectric films. Chung further teaches that the low k organic dielectric films, such as layers 113 and 112 beneath stop layer 114, may have some resistance to pure O_2 plasma. However, Chung does not teach or suggest that stop layer 114 is resistant to a plasma etch. Neither does Chung teach or suggest that stop layer 114 is resistant to plasma including a forming gas. Therefore, the Examiner has not presented a *prima*

facie case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

VIII. CONCLUSION

For the reasons noted above, the rejections of claims 1-3 are in error. Appellants respectfully request reversal of the rejections and allowance of claims 1-6 and 13-18.

Respectfully submitted,
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APPENDIX

1. A method of providing a semiconductor device, the semiconductor device including a first layer desired to be etched, the method comprising the steps of:

(a) providing an anti-reflective coating layer having antireflective properties, wherein the anti-reflective coating layer comprises a layer of SiON having a thickness of less than about 500 Angstroms (Å) deposited on the first layer;

(b) patterning a resist layer, the resist layer including a pattern having a plurality of apertures therein for etching a first portion of the first layer;

(c) etching the first portion of the first layer;

(d) removing the resist layer utilizing a plasma etch, the anti-reflective coating layer being resistant to the plasma etch;

(e) patterning a second resist layer, the second resist layer including a pattern having a plurality of apertures therein for etching a second portion of the first layer; and

(f) etching the second portion of the first layer.

2. The method of claim 1 wherein the anti-reflective coating layer providing step (a) further includes the steps of:

(a1) depositing the anti-reflective coating layer.

3. The method of claim 1 wherein the resist layer removing step (d) further includes the step of:

(d1) performing the plasma etch using a plasma including a forming gas, the anti-reflective coating layer being resistant to the plasma etch using the plasma including the forming gas.

4. A method of providing a semiconductor device, the semiconductor device including a first layer desired to be etched, the method comprising the steps of:

(a) providing an anti-reflective coating layer having antireflective properties, wherein the anti-reflective coating layer comprises a layer of SiON having a thickness of less than about 500 Angstroms (Å) deposited on the first layer;

(b) patterning a resist layer, the resist layer including a pattern having a plurality of apertures therein for etching a first portion of the first layer;

(c) etching the first portion of the first layer;

(d) removing the resist layer utilizing a plasma etch, the anti-reflective coating layer being resistant to the plasma etch;

(e) patterning a second resist layer, the second resist layer including a pattern having a plurality of apertures therein for etching a second portion of the first layer; and

(f) etching the second portion of the first layer;

wherein the resist layer removing step (d) further includes the step of:

(d1) performing the plasma etch using a plasma including a forming gas, the anti-reflective coating layer being resistant to the plasma etch using the plasma including the forming gas;

wherein the plasma further includes four percent of the forming gas.

5. A method of providing a semiconductor device, the semiconductor device including a first layer desired to be etched, the method comprising the steps of:

(a) providing an anti-reflective coating layer having antireflective properties, wherein the anti-reflective coating layer comprises a layer of SiON having a thickness of less than about 500 Angstroms (Å) deposited on the first layer;

(b) patterning a resist layer, the resist layer including a pattern having a plurality of apertures therein for etching a first portion of the first layer;

(c) etching the first portion of the first layer;

(d) removing the resist layer utilizing a plasma etch, the anti-reflective coating layer being resistant to the plasma etch;

(e) patterning a second resist layer, the second resist layer including a pattern having a plurality of apertures therein for etching a second portion of the first layer; and

(f) etching the second portion of the first layer;

wherein the resist layer removing step (d) further includes the step of:

(d1) performing the plasma etch using a plasma including a forming gas, the anti-reflective coating layer being resistant to the plasma etch using the plasma including the forming gas; and

(d2) providing a wet preclean after the plasma etching step (d1).

6. A method of providing a semiconductor device, the semiconductor device including a first layer desired to be etched, the method comprising the steps of:

(a) providing an anti-reflective coating layer having antireflective properties, wherein the anti-reflective coating layer comprises a layer of SiON having a thickness of less than about 500 Angstroms (Å) deposited on the first layer;

(b) patterning a resist layer, the resist layer including a pattern having a plurality of apertures therein for etching a first portion of the first layer;

(c) etching the first portion of the first layer;

(d) removing the resist layer utilizing a plasma etch, the anti-reflective coating layer being resistant to the plasma etch;

(e) patterning a second resist layer, the second resist layer including a pattern having a plurality of apertures therein for etching a second portion of the first layer; and

(f) etching the second portion of the first layer;

wherein a thickness of the SiON anti-reflective coating layer is three hundred Angstroms plus or minus no more than approximately ten percent.

13. A method of providing a semiconductor device including first and second regions having, respectively, first and second types of circuit structures, the method comprising:

depositing a first layer on a substrate;

depositing a layer of SiON on the first layer;

depositing a first resist layer on the SiON layer;

patterning the first resist layer for etching the first layer in the first region of the semiconductor device;

etching the first layer in the first region of the semiconductor device;

removing the first resist layer utilizing a plasma etch;

depositing a second resist layer on the SiON layer;

patterning the second resist layer for etching the first layer in the second region of the semiconductor device;

etching the first layer in the second region of the semiconductor device;

removing the second resist layer; and

removing the SiON layer.

14. The method of claim 13 wherein the SiON layer has a thickness of less than about 500 Angstroms.

15. The method of claim 13 wherein the SiON layer has a thickness of about 300 Angstroms.

16. The method of claim 15 wherein the SiON layer has a thickness of between about 270 and about 300 Angstroms.

17. The method of claim 13 wherein the first type of circuit structure comprises structures for forming memory cells and the second type of circuit structure comprises structures for forming logic circuits.

18. A method for reducing anti-reflective coating layer removal comprising the steps of:

depositing an anti-reflective coating layer on a first layer, wherein said anti-reflective coating layer comprises a layer of SiON having a thickness of less than 500 Angstroms (Å);

patterning a first resist layer on said anti-reflective coating layer, wherein said first resist layer comprises a pattern having a plurality of apertures therein for etching a first portion of said first layer;

etching said first portion of said first layer;

removing said first resist layer utilizing a plasma etch after said first portion of said first layer is etched, wherein said anti-reflective coating layer is resistant to said plasma etch;

patterning a second resist layer, wherein said second resist layer comprises a pattern having a plurality of apertures therein for etching a second portion of said first layer; and

etching said second portion of said first layer.

PTO/SB/17 (11-04)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 10/01/2004. Patent fees are subject to annual revision.

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) **500.00**

Complete if Known	
Application Number	10/079,775
Filing Date	February 12, 2002
First Named Inventor	Plat et al.
Examiner Name	Hsien Ming Lee
Art Unit	2823
Attorney Docket No.	D900D

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order

☑ Deposit Account ☐ None

Deposit Account Number: 01-0365

Deposit Account Name: Advanced Micro Devices, Inc.

The Director is hereby authorized to: (check all that apply)

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FEE CALCULATION

1. BASIC FILING FEE

Fee Description	Fee ($)	Small Entity Fee ($)	Fee Paid($)
Utility Filing Fee	790	395	
Design Filing Fee	350	175	
Plant Filing Fee	550	275	
Reissue Filing Fee	790	395	
Provisional Filing Fee	160	80	

Subtotal (1) $ _____

FEE CALCULATION (continued)

2. EXTRA CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20	50	25
Each independent claim over 3	200	100
Multiple dependent claims	360	180
For Reissues, each claim over 20 and more than in the original patent	50	25
For Reissues, each independent claim more than in the original patent	200	100

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims	Fee ($)	Fee Paid ($)
	_____	_____

Subtotal (2) $ _____

3. OTHER FEES

Fee Description	Fee ($)	Small Entity Fee ($)	Fee Paid($)
1-month extension of time	120	60	
2-month extension of time	450	225	
3-month extension of time	1,020	510	
4-month extension of time	1,590	795	
5-month extension of time	2,160	1,080	
Information disclosure stmt. fee	180	180	
37 CFR 1.17(q) processing fee	50	50	
Non-English specification	130	130	
Notice of Appeal	500	250	
Filing a brief in support of appeal	500	250	500.00
Request for oral hearing	1,000	500	
Other: _____			

Subtotal (3) $ 500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 47.159	Telephone 512.370.2832
Name (Print/Type)	Robert A. Voigt, Jr.		Date March 18, 2005

PTO/SB/21 (09-04)
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TRANSMITTAL FORM

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Total Number of Pages in This Submission: 16

Application Number	10/079,775
Filing Date	February 12, 2002
First Named Inventor	Plat et al.
Art Unit	2823
Examiner Name	Hsien Ming Lee
Attorney Docket Number	D900D

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
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- [ ] Amendment/Reply
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- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
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- [ ] Other Enclosure(s) (please Identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Winstead Sechrest & Minick P.C.		
Signature			
Printed name	Robert A. Voigt, Jr.		
Date	March 18, 2005	Reg. No.	47,159

CERTIFICATE OF TRANSMISSION/MAILING

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Signature	Serena Beller		
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